CLAIMS

1. A microprocessor-based system, comprising at least one peripheral device, and an address map for storing addresses allocated to the or each peripheral device, wherein, when the peripheral device is disabled, the peripheral device is automatically removed from the address map.

2. A microprocessor-based system as claimed in claim 1, comprising a peripheral control register, and further comprising clock generation logic associated with each peripheral device, wherein a peripheral device may be disabled by sending a logic signal from the peripheral control register to the clock generation logic associated with said peripheral device.

3. A microprocessor-based system as claimed in claim 2, wherein, when said logic signal is sent from the peripheral control register to the clock generation logic associated with said peripheral device, a corresponding logic signal is also sent to said address map to remove said peripheral device from the address map.

4. A microprocessor-based system as claimed in claim 1, having a programmable address map, wherein, when the peripheral device is removed from the address map, a clock signal is automatically gated off from the peripheral device.

5. A microprocessor-based system as claimed in claim 1, having a programmable address map, and further comprising clock generation logic associated with each peripheral device, wherein, when the peripheral device is removed from the address map, a logic signal is sent to said clock generation logic to gate off the clock signal from the peripheral device, and thereby disable the peripheral device.

6. A microprocessor-based system as claimed in claim 2, further comprising a clock generator, for supplying a clock signal to each peripheral device, through the associated clock generation logic.

7. A microprocessor-based system as claimed in claim 1, wherein the system is implemented in an integrated circuit, and wherein at least one of the peripheral devices comprises an interface for an external device.

8. A microprocessor-based system as claimed in claim 1, wherein the system is implemented in an programmable logic integrated circuit, and wherein the microprocessor is provided as an embedded device, while at least one of the peripheral device is implemented in programmable logic.

9. An integrated circuit, comprising a microprocessor and at least one peripheral device having a particular functionality, the microprocessor and the or each peripheral device being connected by a bus, and the integrated circuit further comprising an address map for storing addresses allocated to the or each peripheral device to enable accesses thereto over said bus, wherein the processor is able to disable a peripheral device is disabled when the particular functionality thereof is not required, and wherein, when a peripheral device is disabled, said peripheral device is automatically removed from the address map to prevent further access attempts thereto.

10. An integrated circuit as claimed in claim 9, wherein said at least one peripheral device comprises an interface to an external device.

11. An integrated circuit as claimed in claim 9, wherein said at least one peripheral device is implemented in programmable logic.

12. An integrated circuit as claimed in claim 9, further comprising a peripheral control register, and further comprising clock generation logic associated with each peripheral device, wherein a peripheral device may be disabled by sending a logic signal from the peripheral control register to the clock generation logic associated with said peripheral device.

13. An integrated circuit as claimed in claim 12, wherein, when said logic signal is sent from the peripheral control register to the clock generation logic associated with said peripheral device, a corresponding logic signal is also sent to said address map to remove said peripheral device from the address map.

14. An integrated circuit as claimed in claim 12, further comprising a clock generator, for supplying a clock signal to each peripheral device, through the associated clock generation logic.

15. An integrated circuit as claimed in claim 9, wherein said address map is programmable, and wherein, when a peripheral device is removed by said microprocessor from the address map, a clock signal is prevented from reaching said peripheral device to disable said peripheral device.

16. In a microprocessor-based system, comprising at least one peripheral device, and an address map for storing addresses allocated to the or each peripheral device, a method of operation of said system comprising, when the peripheral device is disabled, automatically removing the peripheral device from the address map.

17. A method as claimed in claim 16, wherein said system comprises a peripheral control register, and further comprises clock generation logic associated with each peripheral device, wherein a peripheral device may be disabled by sending a logic signal from the peripheral control register to the clock generation logic associated with said peripheral device, and wherein, when said logic signal is sent from the peripheral control register to the clock generation logic associated with said peripheral device, a corresponding logic signal is also sent to said address map to remove said peripheral device from the address map.

18. A method as claimed in claim 16, wherein the address map is programmable, the method comprising, when a peripheral device is removed from the address map, automatically gating off a clock signal from the peripheral device.

19. A method as claimed in claim 18, wherein said system further comprises clock generation logic associated with each peripheral device, the method comprising, when the peripheral device is removed from the address map, sending a logic signal to said clock generation logic to gate off the clock signal from the peripheral device, and thereby disable the peripheral device.